

400G QSFP-DD SR8 Transceiver Specification

HTQDD-850H-M1BD

Features

- Up to 53.125Gbps data rate per channel by PAM4 modulation
- 8 duplex channels transmitters and receivers
- Integrated 850nm VCSEL array and PD array
- Single MPO-16 connector receptacle optical interface compliant
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable QSFP-DD form factor
- Maximum link length of 100m on 16 core MPO OM4 (MMF) fiber
- Low power dissipation:<10W
- International class 1 laser safety certified
- Operating temperature range: 0°C ~ +70 °C
- Compliant with RoHS10

Applications

- 400GBASE-SR8 Ethernet
- Switch & Router Connections
- Data Centers
- Other 400G Interconnect Requirements.

Standards

- IEEE P802.3cm
- OIF-CEI-04.0
- QSFP-DD MSA
- QSFP-DD-CMIS-Rev4.0

Description

Hirundo's 400G QSFP-DD SR8 Transceiver is designed to transmit and receive serial optical data links up to 53.125 Gb/s data rate (per channel) by PAM4 modulation format over multi-mode fiber. It is a small-form-factor hot pluggable transceiver which is integrated with the high performance VCSEL laser and high sensitivity PIN receiver. It is compliant with 400G Ethernet specs; QSFP-DD MSA.

1. Ordering Information

Table 1.1 Ordering Information

Part No.	Specifications									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Others	
HTQDD-85OH-M1BD	QSFP-DD	400G	VCSEL	-6.5~4dBm	PIN	< -7dBm@ SECQ=0.9dB	0~70 °C	100m	RoHS	400G Base SR8
PN			HTQDD-85OH-M1BD							
Description			400Gbps,MMF,100m,0-70°C							
SAP No			-							
Customer PN			-							

2. Revision History

Table 2.1 Revision History

Version	Initiated	Reviewed	Approved	Date
V1.0	Leo	Virgil	LiuSJ	2020.12.30

3. Absolute Maximum Ratings and Recommended Operating Conditions

Table 3.1 Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	+85
Relative Humidity	RH	%	5	95
Power Supply Voltage	Vcc	V	-0.5	+4.0

Table 3.1 Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	°C	0		70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Bit Rate(Per channel)	BR	GBd		26.5625	

4. Optical Specification

Table 4.1 Optical Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter (per Lane)						
Signaling Speed per Lane		GBd		26.5625		
Modulation format				PAM4		
Center wavelength		nm	840	850	860	
RMS Spectral Width	SW	nm			0.6	
Average Launch Power per Lane	TXPx	dBm	-6.5		4	
Tx OMA per lane	TxOMA	dBm	-4.5		3	
Launch power in OMAouter minus TDECQ(min)		dBm	-5.9			
Optical Extinction Ratio	ER	dB	3			
Optical Return Loss Tolerance	ORL	dB			12	
Encircled Flux	FLX	dBm	>86% at 19um			
			<30%at 4.5um			
Transmitter and dispersion eye closure (TDECQ),each lane		dB			4.5	
Average launch power of OFF Transmitter, each lane		dBm			-30	
RIN ₁₂ OMA					-128	
Receiver(per Lane)						
Signaling Speed per Lane		GBd		26.5625		
Modulation format				PAM4		
Center wavelength		nm	840		860	
Damage Threshold	DT	dBm	5			
Average receive Power per Lane	RXPx	dBm	-8.4		4	
Receive power, each lane (OMAouter)		dBm			3	
Receiver reflectance	Rfl	dB			-12	
Stressed receiver sensitivity(OMAouter),each lane		dBm			-3.4	
LOS De-Assert		dBm			-9	
LOS Asser		dBm	-30		-10	
LOS Hysteresis		dB	0.5			

5. Electrical Specification

Table 5.1 Electrical Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC VCC3.3-Tx VCC3.3-Rx	V	3.135	3.3	3.465	
Power Consumption	Pc	W			10	
Transceiver Power-on Initialize Time		ms			2000	
Transmitter						
Differential peak-to-peak input voltage tolerance		mV			900	
Differential termination mismatch					10%	
Differential input return loss(SDD11)		dB			See CEI-56G -VSR	
Common-mode to differential conversion and differential to common-mode conversion(SCD11,SDC11)		dB			See CEI-56G -VSR	
Receiver						
Differential peak-to-peak output voltage		mV	0		900	
DC Common Mode Voltage	Vcm	mV	-350		2850	
Common Mode Noise, RMS	VcmAC	mV			17.5	
Differential termination mismatch		%			10	
Differential output return loss(SDD22)		dB			See CEI-56G -VSR	
Common-mode to differential conversion and differential to common-mode conversion(SCD22,SDC22)		dB			See CEI-56G -VSR	
IIC communication						
IIC Clock frequency	-	KHz	/	400	1000	
clock stretching	-	us	/	/	500	
Data hold time	-	ns	300	/	/	

6. Module Memory Map

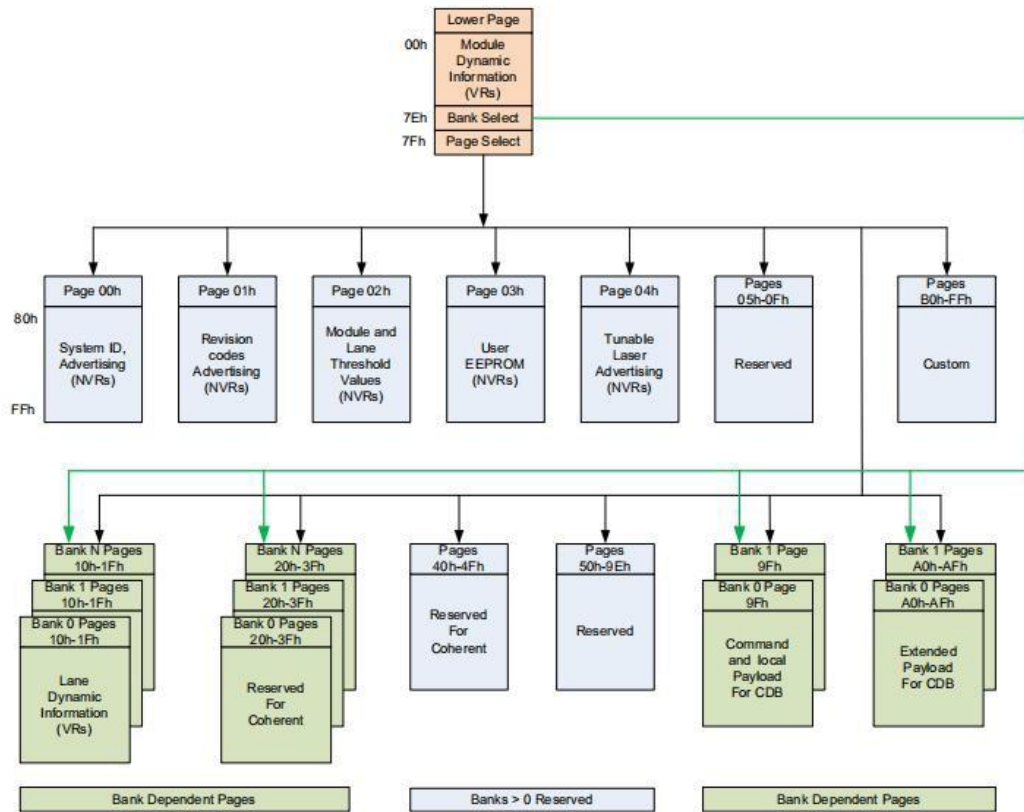


Figure 1 Digital Diagnostic Memory Map

7. Pin Assignment and Pin Description

7.1 Pin Assignment

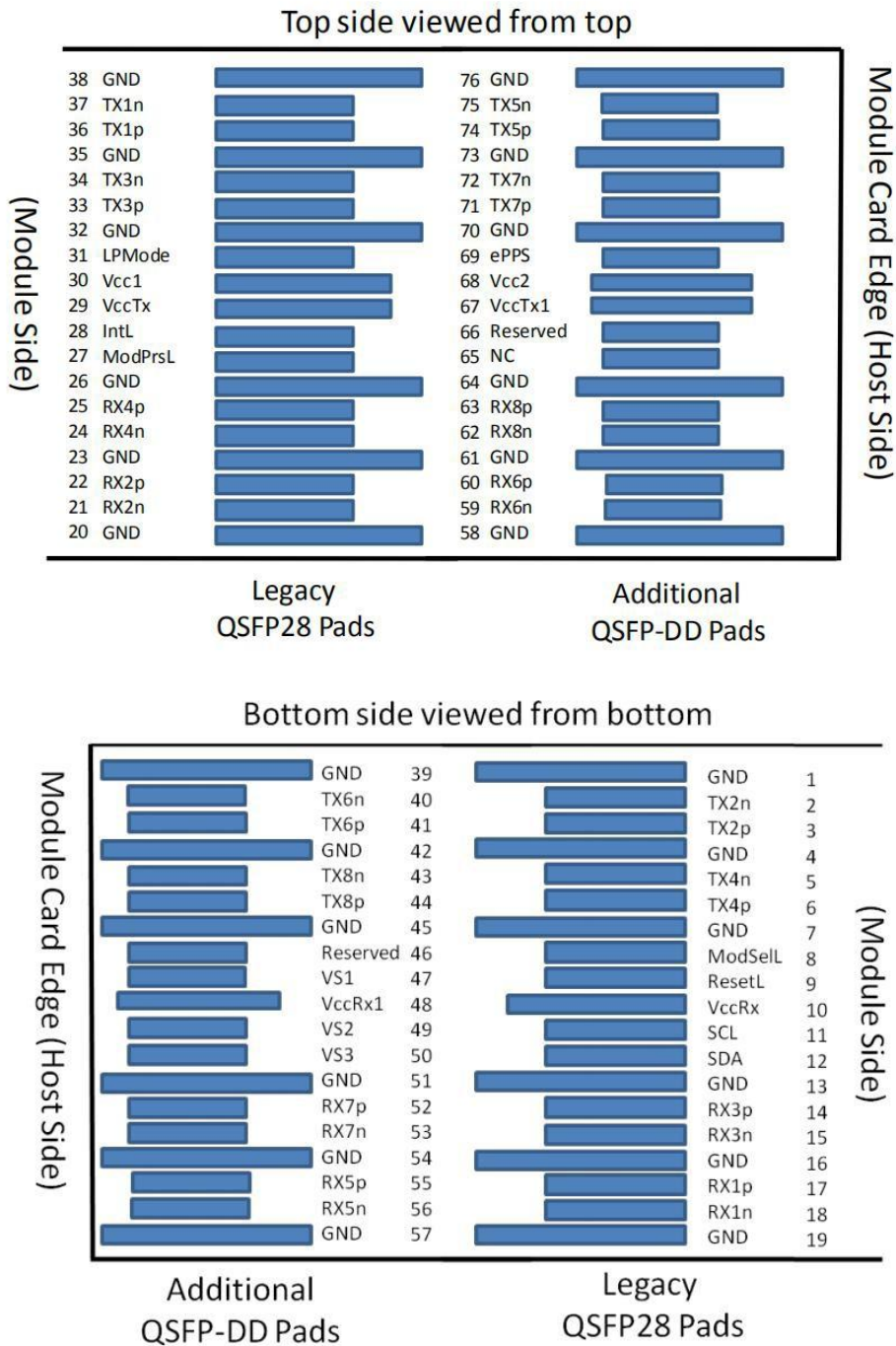


Figure 2. Electrical Pin-out Details

7.2 Pin Description

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	
18	CML-0	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-0	ModPrsL	Module Present	
28	LVTTL-0	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2

Pin	Logic	Symbol	Description	Note
31	LVTTL-I	LPMode	Low Power mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	
37	CML-I	Tx1n	Transmitter Non-Inverted Data output	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data output	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	+3.3V Power Supply Receiver	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	
53	CML-0	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	
56	CML-0	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-0	Rx6n	Receiver Inverted Data Output	
60	CML-0	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1

Pin	Logic	Symbol	Description	Note
62	CML-0	Rx8n	Receiver Inverted Data Output	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For future use	3
67		VccTx 1	+3.3 V Power Supply transmitter	2
68		Vcc2	+3.3 V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Inverted Data Input	
72	CML-I	Tx7n	Transmitter Non-Inverted Data output	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Inverted Data Input	
75	CML-I	Tx5n	Transmitter Non-Inverted Data output	
76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connected these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.

8. Principle diagram

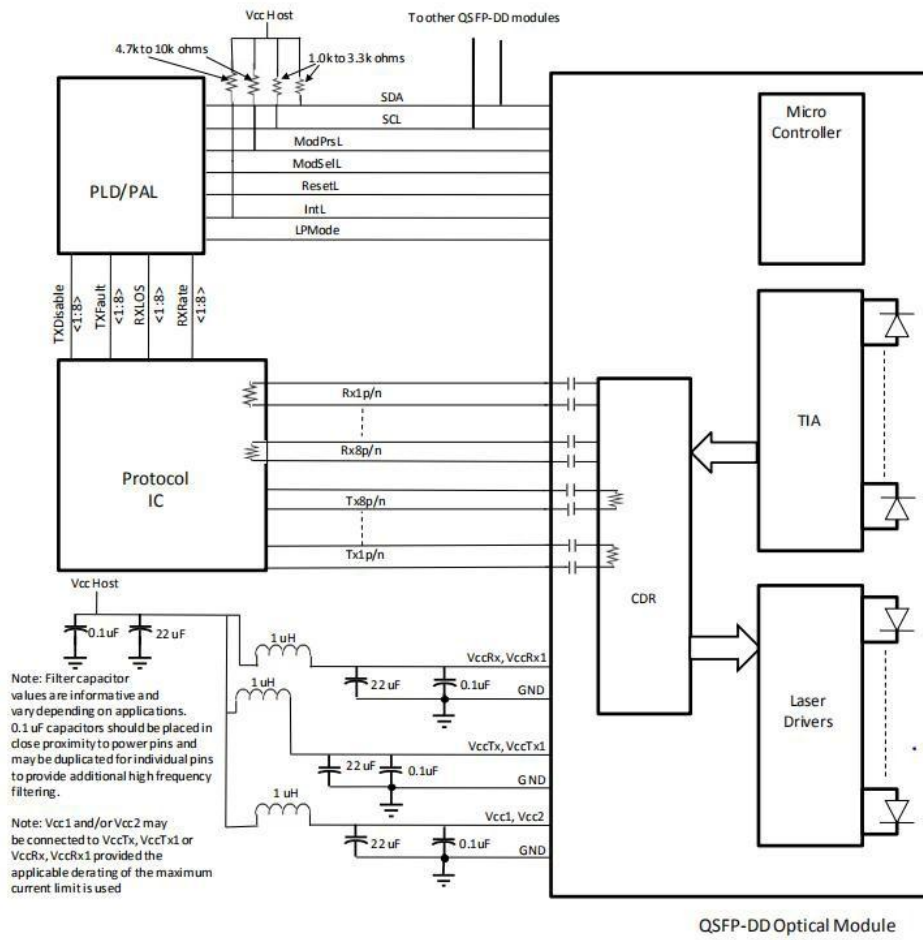


Figure 3. Module Principle Diagram

9. Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

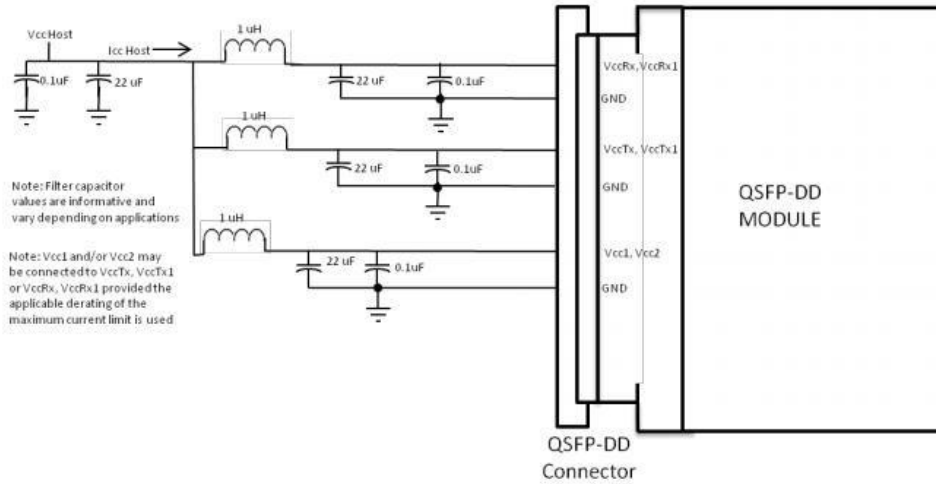


Figure 4 Recommended Host Board Power Supply Filtering

10. Package Outline

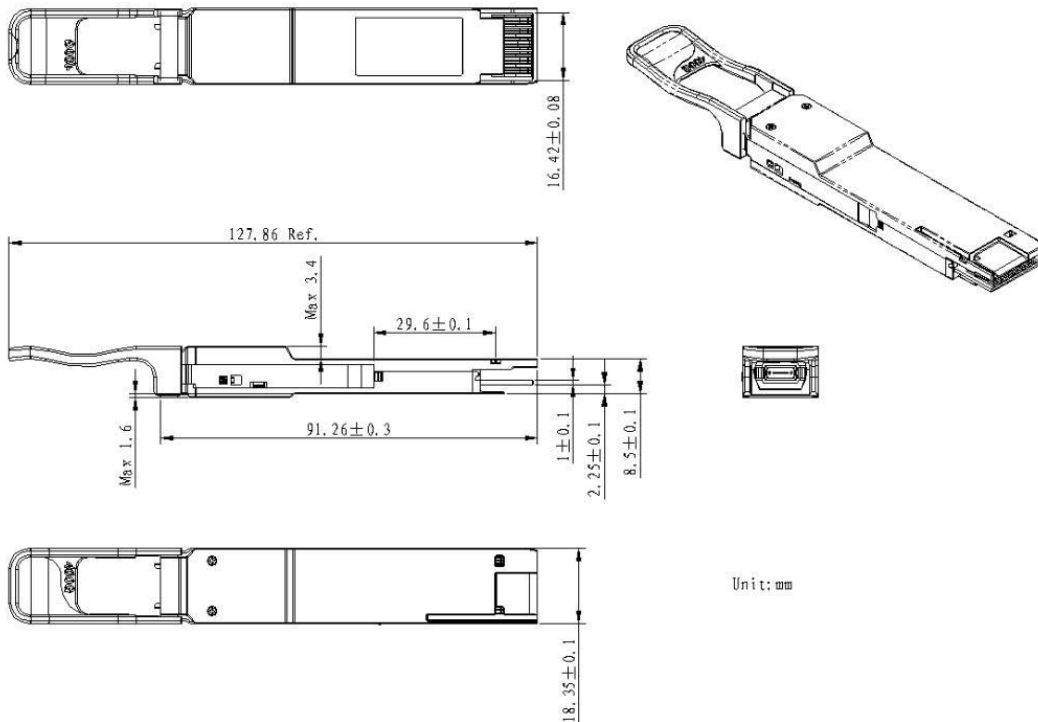


Figure 5 Package Outline

11. Optical Interface

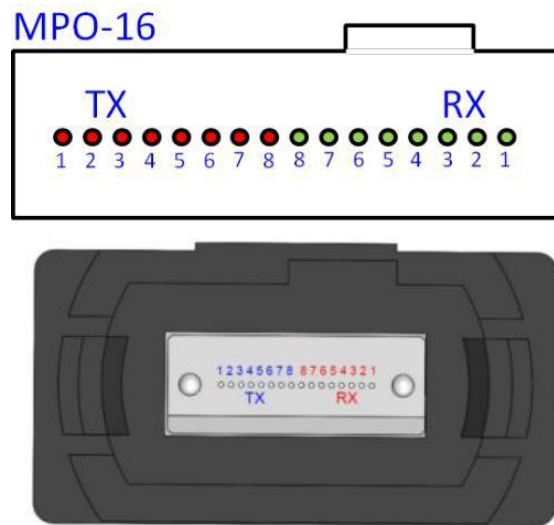


Figure 6. Optical lane sequence

Note: Optical interface is 8°APC MPO-16. Lane sequence is shown in figure 6

12. For More Information

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