

HTXFB-1596-40BD

10Gb/s 40km XFP Optical Transceiver

PRODUCT FEATURES

- Hot-pluggable XFP footprint
- Supports 9.95Gb/s to 11.3Gb/s bit rates
- Supports Lineside and XFI loopback
- RoHS-6 Compliant (lead-free)
- Power dissipation < 3.5W
- Case temperature range:0°C to 70°C
- Maximum link length of 40km
- Cooled 1550nm EML and PIN receiver
- Full Duplex LC connector
- No Reference Clock required
- Built-in digital diagnostic functions
- Standard bail release mechanism

APPLICATIONS

- 10GBASE-ER/EW 10G Ethernet
- 40KM 10G Fiber Channel
- SONET OC-192 &SDH STM 64



PRODUCT DESCRIPTION

Hirundo's HTXFB-1596-40BD Small Form Factor 10 G (XFP) transceivers are compliant with the current XFP Multi-Source Agreement (MSA) Specification. They comply with 10-Gigabit Ethernet 10GBASE-ER/EW per IEEE 802.3ae and 10G Fiber Channel 40KM. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA. The transceiver is RoHS compliant and leads free per Directive 2002/95/EC³.

I. Absolute Maximum Ratings

| Parameter | Symbol | Min | Тур | Max | Unit | NOTE |
|----------------------------|--------|------|-----|-----|------|------|
| Maximum Supply Voltage 1 | Vcc3 | -0.5 | | 4.0 | V | |
| Maximum Supply Voltage 2 | Vcc5 | -0.5 | | 6.0 | V | |
| Storage Temperature | Ts | -40 | | 85 | °C | |
| Case Operating Temperature | Tcase | 0 | | 70 | °C | |

II. Electrical Characteristics

| Parameter | Symbol | Min | Тур | Max | Unit | NOTE |
|--------------------------------|------------------|-----------|-----|--------------|------|------|
| Main Supply Voltage | Vcc5 | 4.75 | | 5.25 | V | |
| Supply Voltage #2 | Vcc3 | 3.13 | | 3.45 | V | |
| Supply Current – Vcc5 supply | Icc5 | | | 320 | mA | |
| Supply Current – Vcc3 supply | Icc3 | | | 450 | mA | |
| Module total power | P | | | 3.5 | W | 1 |
| Transmitter | | | | | | |
| Input differential impedance | Rin | | 100 | | Ω | 2 |
| Differential data input swing | Vin,pp | 120 | | 820 | mV | |
| Transmit Disable Voltage | V_{D} | 2.0 | | Vcc | V | 3 |
| Transmit Enable Voltage | Ven | GND | | GND+ 0.8 | V | |
| Transmit Disable Assert Time | | | | 10 | us | |
| Receiver | | | | | | |
| Differential data output swing | Vout,pp | 340 | 650 | 850 | mV | 4 |
| Data output rise time | t r | | | 38 | ps | 5 |
| Data output fall time | t f | | | 38 | ps | 5 |
| LOS Fault | VLOS fault | Vcc - 0.5 | | Vcchost | V | 6 |
| LOS Normal | VLOS norm | GND | | GND+0.5 | V | 6 |
| Power Supply Rejection | PSR | | See | Note 6 below | | 7 |

Notes:

- 1. Notes: Maximum total power value is specified across the full temperature and voltage range.
- 2. After internal AC coupling.
- 3. Or open circuit.
- 4. Into 100 ohms differential termination.
- 5. These are unfiltered 20-80% values
- 6. Loss Of Signal is open collector to be pulled up with a 4.7k 10kohm resistor to 3.15 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
- 7. Per Section 2.7.1. in the XFP MSA Specification1.

III. Optical Characteristics

| Parameter | Symbol | Min | Тур | Max | Unit | NOTE |
|-----------|--------|-----|-----|-----|------|--------|
| | | | | | | Page 2 |



| Transmitter | | | | | | |
|---|--|-------------------------------------|--|-------|-----|---|
| Average Optical Power | Pout | -1 | | 4 | dBm | |
| Optical Wavelength | λ | 1530 | | 1570 | nm | |
| Side mode Suppression ratio | SMSR | 30 | | | dB | |
| Optical Extinction Ratio | ER | 8.2 | | | dB | |
| Transmitter and Dispersion Penalty | nsmitter and Dispersion Penalty TDP 2 dB | | | | dB | |
| Average Launch power of OFF transmitter | Poff | -30 dBm | | dBm | | |
| Tx Jitter | Txj | Compliant with 802.3ae requirements | | | | |
| Receiver | | | | | | |
| Receiver Sensitivity | Rsens | | | -16.5 | dBm | 1 |
| Input Saturation Power (Overload) | Psat | +0.5 | | | dBm | |
| Wavelength Range | $\lambda_{_{\mathrm{C}}}$ | 1270 | | 1610 | nm | |
| Receiver Reflectance | Rrx | | | -27 | dB | |
| LOS De-Assert | LOSD | | | -18 | dBm | |
| LOS Assert | LOSA | -32 | | | dBm | |
| LOS Hysteresis | | 0.5 | | | dB | |

Notes:

1. Measured with BER $<10^{-12}$ @10.3Gbps,2 31 – 1 PRBS.

IV. Pin Assignment

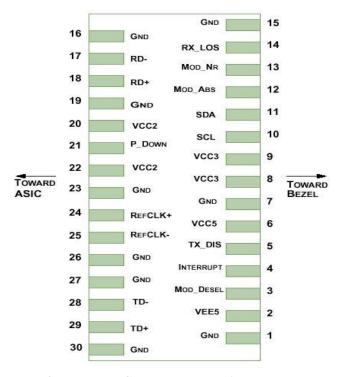


Diagram of Host Board Connector Block Pin Numbers and Name

| Pin | Logic | Symbol | Name/Description | | | |
|-----|-------|--------|---|---|--|--|
| 1 | | GND | Module Ground | 1 | | |
| 2 | | VEE5 | Optional –5.2 Power Supply – Not required | | | |



| LVTTL-I Mod-Desel 2-wire serial interface commands | ond to |
|--|-------------|
| be read over the serial 2-wire interface LVTTL-I | |
| Fower Supply GND | nich can 2 |
| Reference Clock in verted input. AC coupled on the bost bor sequired Petersers Clock in verted input. AC coupled on the bost bor sequired Petersers Clock in verted input. AC coupled on the bost bor sequired Petersers in verted input. AC coupled on the bost bor sequired Petersers in verted input. AC coupled on the bost bor sequired Petersers in verted input. AC coupled on the bost bor sequired Petersers in verted input. AC coupled on the bost bor sequired Petersers inverted input. AC couple | f |
| Serial 2-wire interface clock | |
| 10 | 1 |
| 10 | |
| LVTTL-IO SDA Serial 2-wire interface data line | |
| Module Absent; Indicates module is not present. Grounded module. 13 | 2 |
| 13 | 2 |
| RX_LOS and Loss of Lock in TX/RX. RECEIVER LOS of Signal indicator RX_LOS and Loss of Lock in TX/RX. RECEIVER LOS of Signal indicator RX_LOS and Loss of Lock in TX/RX. RECEIVER LOS of Signal indicator Module Ground RECEIVER INVERTIGE AND ADDRESS OF SIGNAL INTERPRET AND ADDRESS O | in the 2 |
| Module Ground | ween 2 |
| 16 | 2 |
| Receiver inverted data output | 1 |
| 18 CML-O RD+ Receiver non-inverted data output 19 GND Module Ground 20 VCC2 +1.8V Power Supply – Not required 21 LVTTL-I P_Down/RST Power Down; When high, places the module in the low power mode and on the falling edge of P_Down initiates a module Reset; The falling edge initiates a complete reset of the module the 2-wire serial interface, equivalent to a power cycle 22 VCC2 +1.8V Power Supply – Not required 23 GND Module Ground 24 PECL-I RefCLK+ Reference Clock non-inverted input, AC coupled on the host bor required Reference Clock inverted input, AC coupled on the host board. | 1 |
| 19 GND Module Ground 20 VCC2 +1.8V Power Supply – Not required 21 LVTTL-I P_Down/RST Power Down; When high, places the module in the low power mode and on the falling edge of P_Down initiates a module Reset; The falling edge initiates a complete reset of the module the 2-wire serial interface, equivalent to a power cycle 22 VCC2 +1.8V Power Supply – Not required 23 GND Module Ground 24 PECL-I RefCLK+ Reference Clock non-inverted input, AC coupled on the host bor required | |
| VCC2 | |
| 21 LVTTL-I P_Down/RST Power Down; When high, places the module in the low power mode and on the falling edge of P_Down initiates a module Reset; The falling edge initiates a complete reset of the module the 2-wire serial interface, equivalent to a power cycle 22 VCC2 +1.8V Power Supply – Not required 23 GND Module Ground 24 PECL-I RefCLK+ Reference Clock non-inverted input, AC coupled on the host bor required Reference Clock inverted input, AC coupled on the host board. | 1 |
| mode and on the falling edge of P Down initiates a module Reset; The falling edge initiates a complete reset of the module the 2-wire serial interface, equivalent to a power cycle VCC2 +1.8V Power Supply – Not required Module Ground RefCLK+ Reference Clock non-inverted input, AC coupled on the host boar required Reference Clock inverted input, AC coupled on the host boar | |
| Reset; The falling edge initiates a complete reset of the module the 2-wire serial interface, equivalent to a power cycle VCC2 +1.8V Power Supply – Not required Module Ground RefCLK+ Reference Clock non-inverted input, AC coupled on the host bor required Reference Clock inverted input, AC coupled on the host boar | |
| 23 GND Module Ground 24 PECL-I RefCLK+ Reference Clock non-inverted input, AC coupled on the host borequired Reference Clock inverted input, AC coupled on the host board. | |
| 24 PECL-I RefCLK+ Reference Clock non-inverted input, AC coupled on the host borequired Reference Clock inverted input, AC coupled on the host boar | |
| 24 PECL-1 ReICLN+ required Reference Clock inverted input AC counled on the host boar | 1 |
| Reference Clock inverted input AC coupled on the host hoar | ard – Not 3 |
| 25 PECL-I RefCLK- RefCLK- required | 1 – Not 3 |
| 26 GND Module Ground | 1 |
| 27 GND Module Ground | 1 |
| 28 CML-I TD- Transmitter inverted data input | |
| 29 CML-I TD+ Transmitter non-inverted data input | |
| 30 GND Module Ground | 1 |

Notes:

- 1. Module circuit ground is isolated from module chassis ground within the module.
- 2. Open collector; should be pulled up with 4.7k 10kohms on host board to a voltage between 3.15V and 3.6V.
- 3. A Reference Clock input is not required by the HTXFB-1596-40BD. If present, it will be ignored.

V. General Specifications

| Parameter | Symbol | Min | Тур | Max | Units | NOTE |
|-----------------|--------|------|-----|-------|-------|------|
| Bit Rate | BR | 9.95 | | 11.3 | Gb/s | 1 |
| Bit Error Ratio | BER | | | 10-12 | | 2 |



| Max. Supported Link Length | Lmax | | 40 | km | 1 |
|----------------------------|------|--|----|----|---|

Notes:

- 1. 10GBASE-ER/EW.
- 2. Tested with 10.3Gbps, 2³¹ 1 PRBS

VI. Digital Diagnostic Functions

As defined by the XFP MSA, FlyinFiber XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

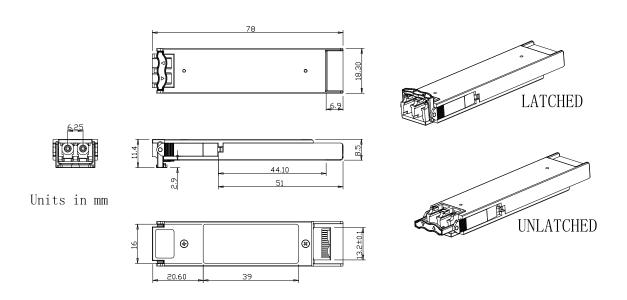
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the XFP MSA Specification.

VII. Mechanical Specifications

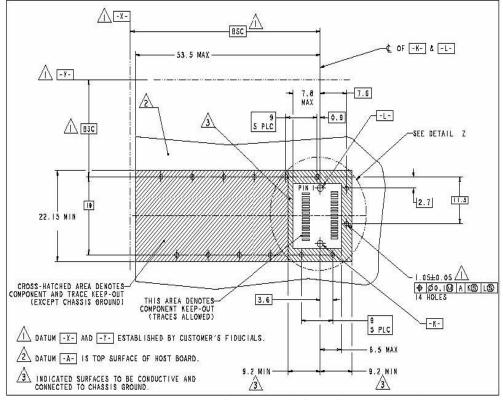
Hirundo's XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).





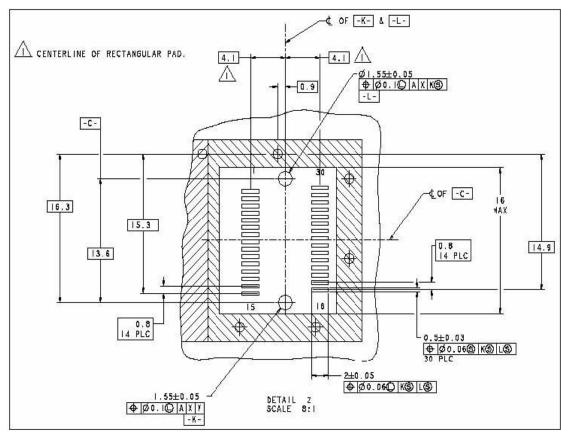
XFP Transceiver (dimensions are in mm)

VIII. PCB Layout and Bezel Recommendations

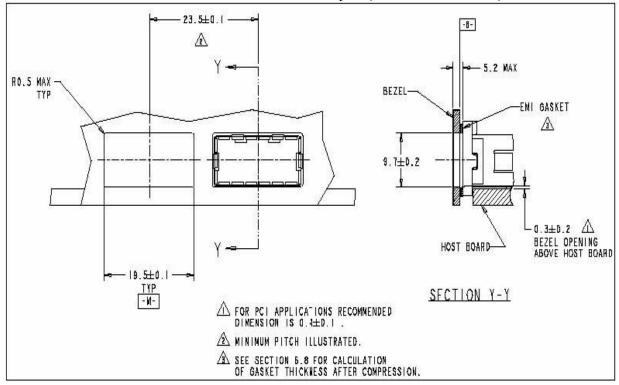


XFP Host Board Mechanical Layout (dimensions are in mm)





XFP Detail Host Board Mechanical Layout (dimensions are in mm)



IX. Regulatory Compliance



| Feature | Reference | Performance | | |
|------------------------------------|---|---------------------------|--|--|
| Electrostatic discharge (ESD) | IEC/EN 61000-4-2 | Compatible with standards | | |
| Electromagnetic Interference (EMI) | FCC Part 15 Class B EN 55022 Class B (CISPR 22A) | Compatible with standards | | |
| Laser Eye Safety | Laser Eye Safety FDA 21CFR 1040.10, 1040.11 IEC/EN 60825-1, 2 | | | |
| Component Recognition | IEC/EN 60950, UL | Compatible with standards | | |
| ROHS | 2002/95/EC | Compatible with standards | | |
| EMC EN61000-3 | | Compatible with standards | | |

Appendix A. Document Revision

| ersion No. | Date | Description | |
|---------------|------------|-----------------------|--|
| 1.0 | 2020-09-01 | Preliminary datasheet | |